DECISION DIRECTED PHASE LOCKED LOOPS (DD-PLL) WITH MULTIPLE INITIAL PHASE AND/OR FREQUENCY ESTIMATES IN DIGITAL COMMUNICATION SYSTEMS

ABSTRACT OF THE DISCLOSURE

A decoder of a data signal subjected to phase shifting keying (PSK) modulation uses an inner decoder for short block codes within a phase locked loop which is adapted to process the data signal with multiple initial phase/frequency error estimates and to output sets of codewords and phase/frequency error estimates respectively corresponding to the initial phase/frequency estimates. A selection circuit (720) selects and forwards the output corresponding to one of the multiple phase/frequency estimates. An outer Reed-Solomon block decoder (319) corrects errors in the codewords from the set of associated codewords selected by the selection circuit.